Amendments to the Specification:

A. Please amend the title to read:

--A SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE MEMORY CELLS WITH LOW RESISTANCE SOURCE REGIONS AND HIGH SOURCE COUPLING--

B. Please amend the first paragraph of the specification as follows:

This is a continuation of U.S. Application 09/916,55, filed June 26, 2001, which ~~[This application]~~ claims the benefit of U.S. Provisional Application No. 60/234,314, filed September 20, 2000, ~~[and entitled Super Self-Aligned Flash EEPROM Cell,]~~ and U.S. Provisional Application No. 60/242,096, filed October 19, 2000, ~~[and entitled Ultra Self-Aligned Flash EEPROM Cell With SAC,]~~ U.S. Provisional Application No. 60/260,167, filed January 5, 2001, ~~[and entitled A Super Self-Aligned Flash E2PROM Cell,]~~ U.S. Provisional Application No. 60/275,517, filed March 12, 2001, ~~[and entitled Super Self-Aligned Flash E2PROM Cell,]~~ and U.S. Provisional Application No. 60/287,047, filed April 26, 2001~~[, and entitled An Ultra Self-Aligned Flash E2PROM Cell With Low Source Resistance and High Source Coupling]~~.

C. Please substitute the paragraph on page 12, lines 4-24 with the following paragraph:

As shown in Fig. 2N, first and second regions 50/80 form the source and drain for each cell (those skilled in the art know that source and drain can be switched during operation). The channel region 92 for each cell is the portion of the substrate that is in-between the source and drain 50/80. Poly blocks 68 constitute the control gate, and poly layer 14 constitutes the floating gate. Oxide layers 32, 36, 46 and 48 together form an insulation layer that is disposed adjacent to and over floating gate 14, to isolate it from [source 96] conductive block 54 and conductive layer 52. Oxide layers 36 and 64 together form an insulation layer that isolates the [source lines 96] conductive block 54 and conductive layer 52 from the control gates 68. The control gates 68 have one side aligned to the edge of the second region 80, and are disposed over part of the channel regions 92. Control gates 68 have lower portions 70 that are disposed adjacent to the

floating gates 14 (insulated therefrom by oxide layer 64), and upper protruding portions 72 that are disposed (extend) over a portion of adjacent poly layers 14 (insulated therefrom by oxide layers 64). A notch 94 is formed by the protruding portion 72, where the sharp edge 66 of floating gate 14 extends into the notch 94. Each floating gate 14 is disposed over part of the channel region 92, is partially overlapped at one end by the control gate 68, and partially overlaps the first region 50 with its other end. Conductive blocks 54 and the conductive layers 52/56 together form source lines 96 that extend across the columns of memory cells. Upper portions 62 of source lines 96 extend over but are insulated from the floating gates 14, while lower portions 60 of source lines 96 are adjacent to but insulated from floating gates 14. As illustrated in the Fig. 2N, the process of the present invention forms pairs of memory cells that mirror each other. The pairs of mirrored memory cells are insulated from other cell pairs by oxide layer 76, nitride spacers 78 and BPSG 86.